Exhibit 10

UNITED STATES DISTRICT COURT
DISTRICT OF MASSACHUSETTS

ACQIS, LLC, Plaintiff, v. EMC CORPORATION, Defendant.	C.A. No. 1:14-cv-13560-ADB

STATEMENT OF MATERIAL FACTS IN SUPPORT OF DEFENDANT EMC CORPORATION'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT

Pursuant to Local Rule 56.1, Defendant EMC Corporation ("EMC") submits this Statement of Material Facts in Support of Its Motion for Summary Judgment of Non-Infringement, showing that there is no genuine issue to be tried.

I. ACQIS's Infringement Allegations

1. Plaintiff ACQIS LLC ("ACQIS") accuses EMC of infringing the following eleven claims ("the asserted claims") from the following eight patents ("the asserted patents"): U.S. Patent No. 7,363,416, claim 60; U.S. Patent No. 7,818,487, claims 38 and 49; U.S. Patent No. 8,041,873, claims 9, 29, and 61; U.S. Patent No. RE41,294, claim 44; U.S. Patent No. RE42,814, claim 31; U.S. Patent No. RE43,119, claim 39; U.S. Patent No. RE43,171, claim 24; and U.S. Patent No. RE44,468, claim 29. Gafford Rpt. (Ex. 1)[1] ¶ 25.

2. ACQIS accuses certain models of EMC's VMAX, VNX, and Isilon products of infringing the asserted patents (hereinafter the "accused products"). Gafford Rpt. (Ex. 1) ¶ 134.

3. ACQIS does not assert infringement under the doctrine of equivalents. Gafford Dep. (5/18/2018) (Ex. 9) at 376:2–6; *see also* Supp. Inf. Cont. (Ex. 15) at 2–11.

4. The accused products communicate between certain system components using PCI Express, not PCI Local Buses. Gafford Rpt. (Ex. 1) ¶¶ 130–31; Gafford Dep. (5/18/2018) (Ex. 9) at 383:10–25.

5. ACQIS alleges that PCI Express communications in the accused products meet the Court's constructions of the limitations related to "PCI bus transaction." Gafford Rpt. (Ex. 1) ¶ 278; *see also generally id.* ¶¶ 210–78; Supp. to Inf. Cont. (Ex. 15) at 2–11.

[1] Exhibits referenced in this Statement of Material Facts are exhibits to the Declaration of Nathan R. Curtis in Support of Defendant EMC Corporation's Motion for Summary Judgment of Non-Infringement, filed concurrently with this Statement.

II. Facts Related to the Lack of a PCI Bus Transaction in the Accused Products

6. Judge Davis in the Eastern District of Texas construed the term "PCI bus transaction" to mean "information, in accordance with the PCI standard, for communication with an interconnected peripheral component." *Markman* Order (D.I. 389) at 6–7.

7. After IPRs concluded on two of the asserted patents, this Court construed the term "PCI bus transaction" to mean "a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component." *Markman* Order (D.I. 389) at 10.

A. Transaction in Accordance with the PCI Local Bus Specification

8. The PCI Local Bus Specification defines transactions to be a particular sequence and content of signals that are exchanged between devices. Hospodor Rpt. (Ex. 4) ¶ 137; Gafford Rpt. (Ex. 1) ¶¶ 50, 54–56; *see generally* PCI Local Bus Spec. (Ex. 12) at 35–55 ("Bus Transactions").

9. Transactions in accordance with the PCI Local Bus Specification are communicated in parallel form. Lindenstruth IPR Decl. (Ex. 5) ¶¶ 60–61, 63; ACQIS IPR Resp. (Ex. 6) at 10 ("The PCI standard specified 32-bit parallel communications.").

10. The Glossary of the PCI Local Bus Specification defines a "transaction" as "[a]n address phase plus one or more data phases." PCI Local Bus. Spec. (Ex. 12) at 272; *see also id.* at 9 ("A bus transaction consists of an address phase followed by one or more data phases.").

11. The Glossary of the PCI Local Bus Specification defines a "phase" as "[o]ne or more clocks in which a single unit of information is transferred, consisting of: an *address phase* (a single address transfer in one clock for a single address cycle and two clocks for a dual address cycle) [and] a *data phase* (one transfer state plus zero or more wait states)." PCI Local Bus. Spec. (Ex. 12) at 271.

12. The PCI Local Bus Specification describes "bus transactions" as including certain control signals, such as FRAME#, IRDY#, and TRDY#, that control the timing and flow of the transaction. PCI Local Bus Spec. (Ex. 12) at 10–11, 25–26, 35–37; '873 patent (Ex. 3) at 22:28–31, Fig. 16; Hospodor Rpt. (Ex. 4) ¶¶ 135, 140, 142; Gafford Rpt. (Ex. 1) ¶ 245.

13. Section 2.2.3 of the PCI Local Bus Specification defines the "Interface Control" signals FRAME#, IRDY#, TRDY#, STOP#, LOCK#, IDSEL, and DEVSEL#. PCI Local Bus Spec. (Ex. 12) at 10–11.

14. The fundamentals of all PCI data transfers are controlled with the FRAME#, IRDY#, and TRDY# control signals. PCI Local Bus Spec. (Ex. 12) at 25.

15. ACQIS's expert, Dr. Lindenstruth, testified in the IPRs that PCI control signals "define the PCI bus transaction" and are "part of what the claims require as a PCI bus transaction." Lindenstruth Dep. (Ex. 11) at 145:18–146:17; *see also id.* at 168:17–169:8 (agreeing that "all of the elements of the PCI bus transaction have to be encoded, including the address, data, [and] control signals").

16. In his validity report in the *IBM* case, Mr. Gafford stated that "an encoded PCI transaction is not just the data in the transaction, but all the PCI signals necessary for the data to be transferred using the PCI bus." Gafford *IBM* Rpt. (Ex. 20) at 83, 99, 167, 188.

17. PCI control signals FRAME#, IRDY#, and TRDY# are necessary for the data to be transferred using the PCI bus. Gafford Dep. (5/3/2018) (Ex. 8) at 80:3–81:7.

18. The PCI Local Bus Specification includes a section titled "Bus Transactions" that describes the timing and content of signals required to effectuate certain bus transaction types, including read and write transactions. PCI Local Bus Spec. (Ex. 12) at 35–3; Hospodor Rpt. (Ex. 4) ¶¶ 141–43.

19. Section 3.3.1 of the PCI Local Bus Specification describes and illustrates the timing and content of signals communicated in a read transaction. PCI Local Bus Spec. (Ex. 12) at 36–37; Hospodor Rpt. (Ex. 4) ¶ 142.

20. Section 3.3.2 of the PCI Local Bus Specification describes and illustrates the timing and content of signals communicated in a write transaction. PCI Local Bus Spec. (Ex. 12) at 37–38; Hospodor Rpt. (Ex. 4) ¶ 143.

21. The read and write transactions shown in the section titled "Bus Transactions" in the PCI Local Bus Specification include the control signals FRAME#, IRDY#, TRDY#, and DEVSEL#. PCI Local Bus Spec. (Ex. 12) at 35–37; Hospodor Rpt. (Ex. 4) ¶¶ 141–43.

22. The read and write transactions shown in the section titled "Bus Transactions" in the PCI Local Bus Specification include an address phase followed by multiple data phases. PCI Local Bus Spec. (Ex. 12) at 35–37; Hospodor Rpt. (Ex. 4) ¶¶ 141–43.

23. The bus transactions described in the PCI Local Bus Specification require a parity bit for each phase of every transaction. Hospodor Rpt. (Ex. 4) ¶¶ 240–41; PCI Local Bus Spec. (Ex. 12) at 10, 95–96; Gafford Dep. (5/3/2018) (Ex. 8) at 111:25–112:18.

24. Parity requires the transmitting device to transmit a single bit that is either a 1 or a 0 so that the total number of 1s on the address/data, command/byte-enable, and parity lines is an even number. PCI Local Bus Spec. (Ex. 12) at 95–96; Gafford Dep. (5/3/2018) (Ex. 8) at 109:22–110:6.

25. According to the PCI Local Bus Specification, parity generation is not optional and must be done by all PCI compliant devices and in every PCI bus transaction. PCI Local Bus Spec. (Ex. 12) at 10, 95.

26. The PCI Local Bus Specification defines specific four-bit bus commands codes that are sent on the C/BE lines during the address phase of a PCI bus transaction. PCI Local Bus Spec. (Ex. 12) at 21; Hospodor Rpt. (Ex. 4) ¶ 207; Gafford Rpt. (Ex. 1) ¶¶ 50–51, 54.

B. Lack of PCI Bus Transactions in the Accused Products

27. There are no transactions in the accused products in which all of the signals set forth in the read transaction defined in Section 3.3.1 of the PCI Local Bus Specification (and not functional equivalents) are actually communicated. Gafford Dep. (5/18/2018) at 398:11–23; *see also id.* at 383:10–25.

28. There are no transactions in the accused products in which all of the signals set forth in the write transaction defined in Section 3.3.2 of the PCI Local Bus Specification (and not functional equivalents) are actually communicated. Gafford Dep. (5/18/2018) at 398:24–399:9; *see also id.* at 383:10–25.

29. None of the interface control signals specified in the PCI Local Bus Specification appear as parallel control signals in any of the accused products. Gafford Dep. (5/18/2018) (Ex. 9) at 469:16–470:6.

30. EMC's accused products do not communicate transactions with *any* of the control signals defined in the PCI Local Bus Specification. Hospodor Rpt. (Ex. 4) ¶¶ 235–39; Gafford Dep. (5/18/2018) (Ex. 9) at 398:11–399:9, 469:16–470:6.

31. Nowhere has ACQIS asserted that the accused products generate or communicate a PCI bus transaction with any of the control signals defined in the PCI Local Bus Specification. *See, e.g.*, Supp. to Inf. Cont. (Ex. 15) at 2–11.

32. Mr. Gafford does not identify any instances in the accused products in which any of the control signals defined in the PCI Local Bus Specification are generated or communicated.

See generally Gafford Rpt. (Ex. 1) ¶¶ 59–77, 103–15, 210–78; Gafford Dep. (5/18/2018) (Ex. 9) at 469:16–470:6.

33. PCI Express does not use any of the control signals defined in the PCI Local Bus Specification. Hospodor Rpt. (Ex. 4) ¶¶ 235–39; Gafford Dep. (5/18/2018) (Ex. 9) at 469:16–470:6; Intro. to PCI Express (Ex. 23) at 81, 180; PCI Express Technology (Ex. 24) at 46, 169.

34. PCI Express does not communicate transactions using phases. Gafford Dep. (5/18/2018) (Ex. 9) at 547:9–12; Hospodor Rpt. (Ex. 4) ¶ 204.

35. The order of information sent over PCI Express in the accused products is not the same as the order required by the PCI Local Bus Specification. Gafford Dep. (5/18/2018) (Ex. 9) at 547:16–549:22.

36. The Expert Report of Thomas A. Gafford does not ever refer to or discuss parity. *See generally* Gafford Rpt. (Ex. 1).

37. PCI Express does not have an error detection mechanism that adds a single parity bit. Gafford Dep. (5/18/2018) (Ex. 9) at 493:13–15; Hospodor Rpt. (Ex. 4) ¶¶ 240–43.

38. PCI Express does not communicate a bit such that the total number of 1s in the address, data, command, byte enable, and parity is an even number. Gafford Dep. (5/18/2018) (Ex. 9) at 493:4–21; Hospodor Rpt. (Ex. 4) ¶¶ 240–43.

39. PCI Express uses a different method than the PCI Local Bus Specification to detect transmission errors. Gafford Dep. (5/18/2018) (Ex. 9) at 493:9–15, 495:10–20, 376:2–6; Hospodor Rpt. (Ex. 4) ¶¶ 240–43.

40. The command bits defined in PCI Express are not in accordance with the PCI Local Bus Specification. Gafford Dep. (5/18/2018) (Ex. 9) at 457:1–19; Hospodor Rpt. (Ex. 4) ¶¶ 208–10.

41. PCI Express packets include a seven-bit code to represent the type of transaction to be performed. Gafford Dep. (5/18/2018) (Ex. 9) at 445:19–25; Hospodor Rpt. (Ex. 4) ¶¶ 208–10.

42. PCI Express does not use the four-bit commands defined in the PCI Local Bus Specification. Gafford Dep. (5/18/2018) (Ex. 9) at 445:19–25; Hospodor Rpt. (Ex. 4) ¶¶ 208–10.

43. A Memory Read transaction in accordance with the PCI Local Bus Specification requires a four-bit command code of "0110," whereas Memory Read Request packet in PCI Express requires a seven-bit code of "0000000." Hospodor Rpt. (Ex. 4) ¶ 210; PCI Local Bus Spec. (Ex. 12) at 21; PCI Express Spec. (Ex. 14) at 53.

44. A Memory Write transaction in accordance with the PCI Local Bus Specification requires a four-bit command code of "0111," whereas a Memory Write Request packet in PCI Express requires a seven-bit code of "1000000." PCI Local Bus Spec. (Ex. 4) at 21; PCI Express Spec. (Ex. 14) at 53.

45. Using the seven-bit PCI Express code for packet type in a PCI Local Bus Specification transaction or using the four-bit PCI Local Bus Specification command code for the packet type in a PCI Express packet would not work. Gafford Dep. (5/18/2018) (Ex. 9) at 446:1-13; 447:8-448:11.

46. ACQIS contends that control signals, address and data phases, and a parity bit are not required parts of a PCI bus transaction in accordance with the PCI Local Bus Specification. Gafford Dep. (5/3/2018) (Ex. 8) at 108:16–21, 158:1–12, 160:2–14; Gafford Dep. (5/18/2018) (Ex. 9) at 426:23–427:13, 455:15–19; PCI Local Bus Spec., as annotated in Gafford Dep. (Ex. 21) at 35–36.

47. ACQIS contends that a PCI bus transaction in accordance with the PCI Local Bus Specification require only address bits, data bits, command bits, and byte enable bits. Gafford

Dep. (5/3/2018) (Ex. 8) at 81:23–83:14; PCI Local Bus Spec., as annotated in Gafford Dep. (Ex. 21) at 36.

III. Facts Related to Lack of Converting PCI Bus Transactions from Parallel to Serial Form in the Accused Products

48. The Court construed the term "encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" and related terms as "a PCI bus transaction that has been serialized from a parallel form." *Markman* Order (D.I. 389) at 16–17.

49. The asserted claims require a PCI bus transaction, beginning in parallel form, to be converted into serial form for transmission across a serial interface. *Markman* Order (D.I. 389) at 16; IPR Hr'g Tr. (Ex. 10) at 32:2–4, 34:14–18, 46:14–47:18; Lindenstruth Dep. (Ex. 11) at 149:20–150:5, 190:23–191:1; Gafford Rpt. (Ex. 1) ¶ 107.

50. PCI Express is a fully serial interface. PCI Express Spec. (Ex. 14) at 31; Gafford Dep. (5/18/2018) (Ex. 9) at 505:2–18.

51. The PCI Express Base Specification Revision 2.0 states: "Key PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its bus implementation is replaced by a highly scalable, fully serial interface." PCI Express Spec. (Ex. 14) at 31.

52. Mr. Gafford does not know whether the accused products first create a PCI bus transaction in parallel form and then convert that into serial form. Gafford Dep. (5/18/2017) (Ex. 9) at 527:1–7.

53. Mr. Gafford does not know whether a PCI bus transaction is ever communicated in parallel form in any of the accused products. Gafford Dep. (5/18/2018) (Ex. 9) at 537:24–538:3.

54. In the context of the asserted patents, the term "parallel" refers to how something is communicated, not how it is stored. Gafford Rpt. (Ex. 1) ¶ 39; Gafford Dep. (5/18/2018) (Ex. 9)

at 378:22–379:14, 646:20–647:2; Lindenstruth IPR Decl. (Ex. 5) ¶ 54; *Markman* Hr'g (Day 2) (Ex. 19) at 199:13–20.

55. The parallel-to-serial converters that ACQIS accuses of serializing a PCI bus transaction from a parallel form receive as their input 10-bit symbols. Hospodor Rpt. (Ex. 4) ¶¶ 259–65.

56. A PCI bus transaction in accordance with the PCI Local Bus Specification must have at least 32 bits of address or data in parallel. ACQIS IPR Resp. (Ex. 6) at 10; *Markman* Order (D.I. 389) at 12, 15.

57. 8b/10b encoding is not parallel-to-serial conversion. *Markman* Hr'g (Day 2) (Ex. 19) at 198:16–24, 203:16–21, 213:18–214:11, 206:12–25, 215:25-216:1, 216:19–217:11, 215:4–14.

58. Breaking up a 32-bit address into four bytes, performing 8b/10b encoding on each byte, and then sending the encoded packets over a serial communication channel is not parallel-to-serial conversion. *Markman* Hr'g (Day 2) (Ex. 19) at 198:16–24, 203:16–21; *see also id.* at 213:18–214:11, 206:12–25, 215:25-216:1, 216:19–217:11, 215:4–14.

IV. Facts Related to Lack of Communicating All Bits of a PCI Bus Transaction in the Accused Products

59. The Court construed the term "communicating . . . PCI bus transaction" and related terms as "communicating a PCI bus transaction, including all address, data, and control bits." *Markman* Order (D.I. 389) at 17–18.

60. ACQIS contends that "control bits" in the Court's construction of the term "communicating . . . PCI bus transaction" refers only to command and byte enable bits. *E.g.*, Gafford Rpt. (Ex. 1) ¶ 239.

61. The asserted patents define a "control bit" as "a data bit that represents a control signal." *E.g.*, '873 patent (Ex. 3) at 17:31–32.

62. The asserted patents describe encoding PCI control signals into serial form, which they call "control bits." '873 patent (Ex. 3) at 17:17–32, 41–60.

63. The '873 patent states: "In the present invention, PCI control signals are encoded into control bits and the control bits rather than the control signals that they represent are transmitted on the interface channel." '873 patent (Ex. 3) at 5:33–36.

64. The asserted patents describe encoding the FRAME# control signal as a control bit to be sent across the serial interface. '873 patent (Ex. 3) at 21:20–21; Gafford Dep. (5/18/2018) (Ex. 9) at 673:20–23; *see also id.* at 407:22–23, 408:4–15; Gafford Dep. (5/3/2018) (Ex. 8) at 164:24–165:3.

65. The asserted patents describe command and byte enable information as corresponding to command and byte enable signals in the PCI Local Bus Specification, and never refer to command or byte enable bits as "control" bits. *E.g.*, '873 patent (Ex. 3) at 20:27–47; *see generally id.*

66. The PCI Local Bus Specification never refers to the command or byte enable bits as "control." Hospodor Rpt. (Ex. 4) ¶ 174; Gafford Dep. (5/18/2018) (Ex. 9) at 449:5–25.

67. The command and byte enable signals are described in the PCI Local Bus Specification as part of the "Address & Data," not as "control." Hospodor Rpt. (Ex. 4) ¶ 174; PCI Local Bus Spec. (Ex. 12) at 7, 9.

68. The accused products do not communicate any bits that are encoded from control signals from a parallel PCI bus transaction. Hospodor Rpt. (Ex. 4) ¶¶ 234–39, 287–97; Gafford Dep. (5/18/2018) (Ex. 9) at 397:4–399:9.

69. The accused products do not communicate any bits that represent control signals from a parallel PCI bus transaction. Hospodor Rpt. (Ex. 4) ¶¶ 234–39, 287–97; Gafford Dep. (5/18/2018) (Ex. 9) at 397:4–399:9.

70. PCI Express does not encode any PCI control signals from a parallel PCI bus transaction into control bits. Hospodor Rpt. (Ex. 4) ¶¶ 234–39, 287–97; Gafford Dep. (5/18/2018) (Ex. 9) at 397:4–399:9.

71. Command and byte enable bits of a PCI Express packet are not encoded PCI control signals. Hospodor Rpt. (Ex. 4) ¶¶ 234–39, 287–97; Gafford Dep. (5/18/2018) (Ex. 9) at 397:4–399:9.

72. Mr. Gafford does not allege that the command and byte enable bits of a PCI Express packet are encoded PCI control signals. *See generally* Gafford Rpt. (Ex. 1).

73. The STP and END symbols in PCI Express are not encoded from the PCI FRAME# control signal. Hospodor Rpt. (Ex. 4) ¶ 289; Gafford Dep. (5/18/2018) (Ex. 9) at 433:18–434:9.

74. The STP symbol in PCI Express is not encoded from the PCI IRDY# control signal. Hospodor Rpt. (Ex. 4) ¶ 293; *see also* Gafford Dep. (5/18/2018) (Ex. 9) at 433:18–434:9.

75. The STP symbol in PCI Express is not encoded from the PCI TRDY# control signal. Hospodor Rpt. (Ex. 4) ¶ 296; *see also* Gafford Dep. (5/18/2018) (Ex. 9) at 433:18–434:9.

76. Flow control credits in PCI Express are not encoded from the PCI IRDY# control signal. Hospodor Rpt. (Ex. 4) ¶ 295; *see also* Gafford Dep. (5/18/2018) (Ex. 9) at 433:18–434:9, 484:6–25.

77. Flow control credits in PCI Express are not encoded from the PCI TRDY# control signal. Hospodor Rpt. (Ex. 4) ¶ 294; *see also* Gafford Dep. (5/18/2018) (Ex. 9) at 433:18–434:9, 484:6–25.

Dated: July 19, 2018

Respectfully submitted,

/s/ Josh Krevitt

OF COUNSEL:

GIBSON, DUNN & CRUTCHER LLP

Josh Krevitt
Benjamin Hershkowitz
Paul E. Torchia
Brian A. Rosenthal
Katherine Q. Dominguez
Laura Corbin
200 Park Avenue
New York, NY 10166-0193
Telephone: (212) 351-4000
jkrevitt@gibsondunn.com
bhershkowitz@gibsondunn.com
ptorchia@gibsondunn.com
kdominguez@gibsondunn.com
lcorbin@gibsondunn.com

Jordan Bekier
333 S. Grand Ave.
Los Angeles, CA 90071-3197
Telephone: (213) 229-7000
jbekier@gibsondunn.com

Nathan Curtis
2100 McKinney Avenue, Suite 1100
Dallas, TX 75201-6912
Telephone: (214) 698-3100
ncurtis@gibsondunn.com

Michael J. Connolly (BBO #638611)
Christine K. Bush (BBO #635381)
John A. Gallagher (BBO #658647)
Hinckley, Allen & Snyder LLP
28 State Street
Boston, MA 02109
Telephone: (617) 345-9000
mconnolly@hinckleyallen.com
cbush@hinckleyallen.com
jgallagher@hinckleyallen.com

Krishnendu Gupta (BBO #632793)
Thomas A. Brown (BBO #657715)
EMC Corporation
176 South Street
Hopkinton, MA 01748
krish.gupta@emc.com
tom.brown@emc.com

Attorneys for Defendant EMC Corporation

CERTIFICATE OF SERVICE

I, Josh Krevitt, hereby certify that on this 19th day of July, 2018, I caused true and accurate copies of the within document to be served on all counsel who have requested notice in this case via the Court's CM/ECF system.

/s/Josh Krevitt
Josh Krevitt